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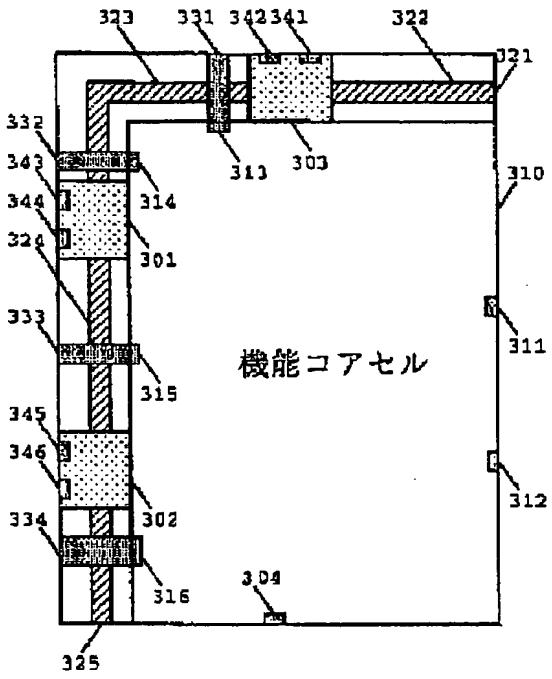
TITLE : ARRANGEMENT METHOD OF BOUNDARY SCAN REGISTER IN SEMICONDUCTOR INTEGRATED CIRCUIT



ABSTRACT : PROBLEM TO BE SOLVED: To prevent a wiring from increasing in length so as not to cause a deterioration in signal or timing to induce a quality trouble in a semiconductor integrated circuit which comprises boundary scan registers and a functional core to realize a test of ANSI/IEEE 1149.1 standard.

SOLUTION: A region where boundary scan register cells 301 to 303 are arranged is provided to the adjacent sides of the I/O circuit cell of a functional core cell 310, the boundary scan register cells 301 to 303 are arranged confronting the I/O circuit cell to form a functional cell where the input/output pins 331 to 334 of the functional core cell and the input/output pins 341 to 346 of the boundary scan register cells are made to serve as outside input/output pins, and the functional cell is arranged on a chip, whereby boundary scan register cells are arranged adjacent to an I/O circuit cell.